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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,694	02/28/2002	Gary J. Kovar	SC11763TK	1627

23125 7590 09/05/2003

MOTOROLA INC
AUSTIN INTELLECTUAL PROPERTY
LAW SECTION
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EXAMINER
ANDUJAR, LEONARDO

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/085,694	KOVAR ET AL.	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *22-31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,11-14,17,18,20 and 21* is/are rejected.

7)☒ Claim(s) *5,7-10,15,16 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I, claims 1-21 in Paper No. 5 is acknowledged. The traversal is on the ground(s) that the subject matter of claims 1-31 is sufficiently related that a thorough and complete search for the subject matter of the elected claims would necessarily encompass a thorough and complete search for the subject matter of the non-elected claims. This is not found persuasive because referring to the restriction requirement set forth in the Office Action paper no. 3, it clearly shows that the process of using the product as claimed can be practiced with another materially different product. Additionally, the search is not coextensive as evidenced by the different fields of search for the process and product as cited in the previous restriction requirement. Furthermore, Applicant has not provided a convincing argument that the product of using can be practiced with another materially different product. Note that the unpatentability of the Group I invention would not necessarily imply unpatentability of the Group II invention. Thus the requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4, 6, 11-14, 17, 18, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moden (US 6,551,845) in view of Kwon (US 6,251,695).

4. Regarding claim 1, Moden (e.g. fig. 3) shows most aspects of the instant invention including a method for testing a plurality of semiconductor die, wherein the method comprises:

- Providing a of semiconductor die 2;
- Encapsulating the semiconductor die (col. 1/lls. 30-43);
- Placing the semiconductor on a temporary substrate 30;
- Placing the semiconductor with the temporary substrate on a testing platform 10;
- Testing the of semiconductor die while it is on the temporary substrate and the testing platform;
- And removing the temporary substrate.

5. However Moden does not show the step of providing a plurality of semiconductor dies to form an array. Kwon (e.g. fig. 2) discloses a method of testing a plurality of semiconductor dies including the step of providing a plurality of semiconductor dies and encapsulating a plurality of semiconductor dies to form an array, wherein the array has a perimeter. Kwon discloses that the multi chip module packaging technology (i.e. an encapsulated array of semiconductors) has the advantage of shortening circuit design time because the designer is not constrained to design the entire target circuit or fabricated the entire target circuit on a single silicon die (col. 1/lls. 52-58). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of forming a multi chip package or to include the step of providing a

plurality of semiconductor dies and encapsulating a plurality of semiconductor dies to form an array, wherein the array has a perimeter in order to reduce the circuit design time because the designer is not constrained to design the entire target circuit or fabricated the entire target circuit on a single silicon die as taught by Kwon. In this case, the semiconductor die array disclosed by Kwon substitutes the single die disclosed by Moden.

6. Regarding claim 2, Moden shows that the temporary substrate is a temporary adhesive substrate (abstract).

7. Regarding claim 3, Kwon shows that a support structure outside the perimeter of the array (e.g. solder balls).

8. Regarding claim 4, Moden shows that the temporary substrate comprises a support structure.

9. Regarding claim 6, Kwon shows that the plurality of semiconductor dies are attached to a package substrate 54 and electrically connected to package substrate (see fig. 2).

10. Regarding claim 11, Kwon shows that the step of encapsulating the plurality semiconductor dies further comprises molding the plurality of semiconductor dies (see figure 2).

11. Regarding claim 12, Kwon shows that the semiconductor dies can be tested in parallel. Note that the first die is tested before the second die.

12. Regarding claim 13, Moden (e.g. fig. 3) shows most aspects of the instant invention including a method for testing a plurality of semiconductor die, wherein the method comprises:

- Placing a semiconductor die 2 on a temporary adhesive substrate 30;
- Placing the semiconductor die with the temporary adhesive substrate on a testing platform 10;
- Testing the semiconductor die;
- And removing the temporary adhesive substrate after testing.

13. However Moden does not show the steps of providing a semiconductor wafer, singulating the semiconductor wafer to form a plurality of semiconductor dies and providing a plurality of semiconductor dies to form an array. Kwon discloses a method of testing a plurality of semiconductor dies including the steps of providing a semiconductor wafer, singulating the semiconductor wafer to form a plurality of semiconductor dies (e.g. fig. 1); and forming an array of semiconductor dies (e.g. fig. 2). Kwon discloses that the multi chip module packaging technology (i.e. the semiconductor die array) has the advantage of shortening circuit design time because the designer is not constrained to design the entire target circuit or fabricated the entire target circuit on a single silicon die (col. 1/lls. 52-58). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of forming a multi chip package or to include the steps of providing a semiconductor wafer, singulating the semiconductor wafer to form a plurality of semiconductor dies and forming an array of a plurality of semiconductor dies in order to reduce the circuit design time because the

designer is not constrained to design the entire target circuit or fabricated the entire target circuit on a single silicon die as taught by Kwon. In this case, the semiconductor die array disclosed by Kwon substitutes the single die disclosed by Moden.

14. Regarding claim 14, Kwon shows that the plurality of semiconductor dies are attached to a package substrate 54 and electrically connected to package substrate (see fig. 2).

15. Regarding claim 17, Kwon shows that the plurality of semiconductor dies are encapsulated. Also, the array includes a perimeter.

16. Regarding claim 18, Kwon shows a support structure 10 that is in contact with the temporary adhesive substrate.

17. Regarding claim 20, Moden in view of Kwon shows that the array includes the plurality of semiconductor dies. Also, the array is placing prior to placing the plurality of semiconductor dies on the temporary adhesive substrate.

18. Regarding claim 21, Moden in view of Kwon shows that the plurality of semiconductor dies on the temporary adhesive substrate form an array.

Allowable Subject Matter

19. Claims 5, 7-10, 15, 16 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

20. Papers related to this application may be submitted directly to Art Unit 2826 by facsimile transmission. Papers should be faxed to Art Unit 2826 via the Art Unit 2826

Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2826 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2826 Fax Center is to be used only for papers related to Art Unit 2826 applications.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Leonardo Andújar** at **(703) 308-0080** and between the hours of 9:00 AM to 7:30 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Leonardo.Andujar@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn, can be reached on (703) 308-6601.

22. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 305-3900.**

23. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass (es): 438/14, 15; 257/685	08/03
Other Documentation:	
Electronic Database(s): East (USPAT, US PGPUB, JPO, EPO, Derwent, IBM TDB)	08/03

Leonardo Andújar
Patent Examiner Art Unit 2826
LA
8/20/03

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